10/027911

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Richard T. IDA, et al.

Assignee: Freescale Semiconductor, Inc.

Title: SEMICONDUCTOR APPARATUS

Patent No.: 6,936,896 B2 Issued: August 30, 2005

Atty. Docket No.: 1280-SC11963ZC

Mail Stop Certificate of Correction Branch
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REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT— PTO MISTAKE (37 C.F.R. § 1.322(a))

Dear Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322(a), please issue a Certificate of Correction in the above-identified matter. The mistake(s) to be corrected was made by the Office.

1. Attached hereto, in duplicate, is Form PTO-1050, with at least one copy suitable for printing.
2. The exact page(s) and line number(s) where the error(s) is shown correctly in the application file:
   Amendment After Allowance (see page 6) attached hereto.
3. Please send the Certificate to:

   J. Gustav Larson
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   5000 PLAZA ON THE LAKE, SUITE 265
   AUSTIN, TX 78746

Respectfully submitted,

10-8-05
Date

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,936,896 B2

DATED : August 30, 2005

INVENTOR(S) : Richard T. IDA, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 7

Line 22, add --wherein-- after Claim 1

Column 7

Line 9, change Claim "9" to Claim --1--

MAILING ADDRESS OF SENDER:

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PATENT NO. 6,936,896 B2

No. of additional copies

OCT 21 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Richard T. Ida et al.		
Title:	SEMICONDUCTOR APPARATUS		
App. No.:	10/027,911	Filed:	12/21/2001
Examiner:	Jerome Jackson, Jr.	Group Art Unit:	2815
Atty. Dkt. No.:	1280.SC11963ZC		

Mail Stop Issue Fee
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER ALLOWANCE (37 C.F.R. § 1.312)

Dear Sir:

This Amendment is being submitted following the Notice of Allowance mailed on October 12, 2004 and prior to payment of the issue fee.

Claim Amendments begin on page 2.

Remarks begin on page 12.

CERTIFICATE OF TRANSMISSION/MAILING
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to the Commissioner for Patents on 10/13/05.

Typed or Printed Name

Signature

Claim Amendments

Please amend claims 27 and 43 as indicated.

1. – 17. (Canceled)

18. (Previously Presented) An integrated data processing device comprising:

a first circuit coupled to a first voltage reference node;

a second circuit coupled to a second voltage reference node;

an electrostatic discharge protection device operable to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event, the electrostatic discharge protection device comprising

a first conductivity type junction formed between a first region of a first conductivity type and a second region of a second conductivity type;

a second conductivity type junction formed between the second region and a third region of the first conductivity type;

a third conductivity type junction formed between the third region and a fourth region of the second conductivity type, the fourth region coupled to the second voltage reference node; and

an anode node coupled to the first voltage reference node and connected to one or more regions of the electrostatic discharge protection device including the first region, wherein all regions of the discharge protection device connected to the anode node are of a common conductivity type; and

a low voltage trigger control portion coupled to the second region and the third region to provide a electrostatic discharge protection device triggering current at a voltage of less than 10 volts.

19. (Canceled)

20. (Canceled)

21. (Previously Presented) An apparatus comprising:

a first circuit coupled to a first voltage reference node;

a second circuit coupled to a second voltage reference node;

an electrostatic discharge protection device operable to provide a current path and a capacitance of less than 120 Femtofarads between the first voltage reference node and the second voltage reference node during an electrostatic event, the electrostatic discharge protection device comprising

a thyristor coupled between the first voltage reference node and the second voltage reference node to provide the current path.

22. (Canceled)

23. (Previously Presented) The apparatus of claim 21 wherein the first circuit is an analog circuit and the second circuit is a digital circuit.

24. (Previously Presented) The apparatus of claim 21 wherein the first circuit is a radio frequency analog circuit.

25. (Previously Presented) The apparatus of claim ~~23~~ 24 wherein the second circuit is a digital circuit.

26. (Previously Presented) The apparatus of claim 24 wherein the second circuit is an analog circuit.

27. (Currently Amended) A method comprising ~~the steps of~~:

providing a voltage reference to a first circuit of an integrated circuit device using a first voltage reference node during normal operation;

providing the voltage reference to a second circuit of the integrated circuit device using a second voltage reference node during normal operation, the second voltage reference node and the first voltage reference node being different nodes;

detecting a voltage difference between the first voltage reference node and the second voltage reference node of less than approximately 10 volts to determine when an electrostatic discharge event is occurring; and

providing a conductive path through a thyristor having a capacitance of less than 120 Femtofarads from anode to cathode when the voltage difference is detected.

28. (Canceled)

29. (Previously Presented) The method of claim 27, wherein the voltage difference is less than 10 volts.

30. (Canceled)

31. (Canceled)

32. (Canceled)

33. (Previously Presented) An apparatus comprising:

a thyristor comprising

a plurality conductivity type junctions comprising

a first conductivity type junction formed between a first region of a first conductivity type and a second region of a second conductivity type;

a second conductivity type junction formed between the second region and a third region of the first conductivity type;

a third conductivity type junction formed between the third region and a fourth region of the second conductivity type;

a voltage trigger control coupled to the second region and the third region to provide a thyristor triggering current at a voltage of less than 10 volts;

an anode connected to the plurality of conductivity type junctions only at the first region;

a cathode coupled to the fourth region;

a first voltage reference node coupled to a first circuit and the anode; and

a second voltage reference node coupled to a second circuit and the cathode, wherein the thyristor is operable to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event.

34. (Previously Presented) The apparatus of claim 33 wherein the second region is a well region of the second conductivity type.

35. (Previously Presented) The apparatus of claim 34 wherein the third region is a well region of the first conductivity type.

36. (Previously Presented) The apparatus of claim 35, wherein the cathode is connected to the plurality of conductivity type junctions only at the fourth region.

37. (Previously Presented) The apparatus of claim 33, wherein the cathode is connected to the plurality of conductivity type junctions only at the fourth region.

38. (Previously Presented) The apparatus of claim 33, wherein the first voltage reference node and the second reference node are to provide a common voltage reference.

39. (Canceled)

40. (Previously Presented) The apparatus of claim 33, wherein the voltage trigger control is a zener diode.

41. (Previously Presented) The apparatus of claim 33, wherein the voltage trigger control is a field effect transistor.

42. (Previously Presented) The apparatus of claim 18, wherein the first voltage reference node and the second voltage reference node are ground nodes.

43. (Currently Amended) The device of claim 42, wherein the electrostatic discharge protection device further comprises:

[[and]]a cathode node coupled to the second voltage reference node and connected to one or more regions of the electrostatic discharge protection device including the fourth region, wherein all regions of the electrostatic discharge protection device connected to the anode node are of a common conductivity type.

44. (Previously Presented) The apparatus of claim 18 wherein the first circuit is an analog circuit and the second circuit is a digital circuit.

45. (Previously Presented) The apparatus of claim 44 wherein the second circuit is a digital circuit.

46. (Previously Presented) The apparatus of claim 18 wherein the first circuit is a radio frequency analog circuit.

47. (Previously Presented) The apparatus of claim 46 wherein the second circuit is an analog circuit.

48. (Previously Presented) The apparatus of claim 18, wherein the low voltage trigger control portion is a zener diode.

49. (Previously Presented) The apparatus of claim 18, wherein the low voltage trigger control portion is a field effect transistor.

50. (Previously Presented) An integrated data processing device comprising:

a first circuit coupled to a first voltage reference node;

a second circuit coupled to a second voltage reference node;

an electrostatic discharge protection device operable to provide a current path and a capacitance of less than 120 Femtofarads between the first voltage reference node and the second voltage reference node during an electrostatic event, the electrostatic discharge protection device comprising

a first conductivity type junction formed between a first region of a first conductivity type and a second region of a second conductivity type;

a second conductivity type junction formed between the second region and a third region of the first conductivity type;

a third conductivity type junction formed between the third region and a fourth region of the second conductivity type, the fourth region coupled to the second voltage reference node; and

an anode node coupled to the first voltage reference node and connected to one or more regions of the electrostatic discharge protection device including the first region, wherein all regions of the discharge protection device connected to the anode node are of a common conductivity type.

51. (Previously Presented) The apparatus of claim 51 wherein the first circuit is an analog circuit and the second circuit is a digital circuit.

52. (Previously Presented) The apparatus of claim 50a wherein the second circuit is a digital circuit.

53. (Previously Presented) The apparatus of claim 53 wherein the first circuit is a radio frequency analog circuit.

54. (Previously Presented) The apparatus of claim 50b wherein the second circuit is an analog circuit.

55. (Previously Presented) An apparatus comprising:
a first circuit coupled to a first voltage reference node;
a second circuit coupled to a second voltage reference node;
an electrostatic discharge protection device operable to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event, the electrostatic discharge protection device comprising
a thyristor coupled between the first voltage reference node and the second voltage reference node to provide the current path, the thyristor comprising a voltage trigger control portion coupled to provide a thyristor triggering current at a voltage of less than 10 volts.

56. (Previously Presented) The apparatus of claim 55 wherein the first circuit is an analog circuit and the second circuit is a digital circuit.

57. (Previously Presented) The apparatus of claim 56 wherein the second circuit is a digital circuit.

58. (Previously Presented) The apparatus of claim 55 wherein the first circuit is a radio frequency analog circuit.

59. (Previously Presented) The apparatus of claim 58 wherein the second circuit is an analog circuit.

60. (Previously Presented) The apparatus of claim 55, wherein the voltage trigger control portion is a zener diode.

61. (Previously Presented) The apparatus of claim 55, wherein the voltage trigger control portion is a field effect transistor.

62. (Previously Presented) The apparatus of claim 27 wherein the first circuit is an analog circuit and the second circuit is a digital circuit.

63. (Previously Presented) The apparatus of claim 62 wherein the second circuit is a digital circuit.

64. (Previously Presented) The apparatus of claim 27 wherein the first circuit is a radio frequency analog circuit.

65. (Previously Presented) The apparatus of claim 64 wherein the second circuit is an analog circuit.

66. (Previously Presented) The apparatus of claim 33 wherein the first circuit is an analog circuit and the second circuit is a digital circuit.

67. (Previously Presented) The apparatus of claim 66 wherein the second circuit is a digital circuit.

68. (Previously Presented) The apparatus of claim 33 wherein the first circuit is a radio frequency analog circuit.

69. (Previously Presented) The apparatus of claim 68 wherein the second circuit is an analog circuit.

70. (Previously Presented) The apparatus of claim 33, wherein the voltage trigger control is a zener diode.

71. (Previously Presented) The apparatus of claim 33, wherein the voltage trigger control is a field effect transistor.

72. (Previously Presented) An apparatus comprising:

a thyristor operable to provide a current path from a first region to a fourth region having

a capacitance of less than 120 Femtofarads comprising

a plurality conductivity type junctions comprising

a first conductivity type junction formed between the first region of a first conductivity type and a second region of a second conductivity type;

a second conductivity type junction formed between the second region and a third region of the first conductivity type;

a third conductivity type junction formed between the third region and the fourth region of the second conductivity type;

an anode connected to the plurality of conductivity type junctions only at the first region;

a cathode coupled to the fourth region;

a first voltage reference node coupled to a first circuit and the anode; and

a second voltage reference node coupled to a second circuit and the cathode, wherein the thyristor is operable to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event.

73. (Previously Presented) The apparatus of claim 72 wherein the second region is a well region of the second conductivity type.

74. (Previously Presented) The apparatus of claim 73 wherein the third region is a well region of the first conductivity type.

75. (Previously Presented) The apparatus of claim 74, wherein the cathode is connected to the plurality of conductivity type junctions only at the fourth region.

76. (Previously Presented) The apparatus of claim 72, wherein the cathode is connected to the plurality of conductivity type junctions only at the fourth region.

77. (Previously Presented) The apparatus of claim 72, wherein the first voltage reference node and the second reference node are to provide a common voltage reference.

78. (Previously Presented) The apparatus of claim 72 further comprising:

a voltage trigger control coupled to the second region and the third region to provide a thyristor triggering current.

79. (Previously Presented) The apparatus of claim 78, wherein the voltage trigger control is a zener diode.

80. (Previously Presented) The apparatus of claim 78, wherein the voltage trigger control is a field effect transistor.

81. (Previously Presented) The apparatus of claim 72 wherein the first circuit is an analog circuit and the second circuit is a digital circuit.

82. (Previously Presented) The apparatus of claim 81 wherein the second circuit is a digital circuit.

83. (Previously Presented) The apparatus of claim 72 wherein the first circuit is a radio frequency analog circuit.

84. (Previously Presented) The apparatus of claim 83 wherein the second circuit is an analog circuit.

REMARKS

Claims 27 and 43 have been amended to address various informalities. The amendments to the claims do not change the scope of the claims. Entry thereof is therefore respectfully requested.

Should the Examiner deem that any further action by the Applicants would be desirable for placing this application in even better condition for issue, a call to the Applicants' representative listed below is requested.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

Date: 1/3/05

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